# FPGA Implementation of Low Power, High Speed, Area Efficient Invisible Image Watermarking Algorithm for Images

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**Abstract**— In recent years, the applications about multimedia have been developed rapidly. Due to rapid development in the network and communication field, it has become necessary to protect the data during transmission. Digital watermarking is a solution to the copyright protection and authentication of data in the network. Protection of digital multimedia content has become an increasingly important issue for content owners and service providers. So there has been growing interest in developing effective techniques to discourage the unauthorized duplication of digital data In this technique, based Image robust watermarking technique for color and gray scale images was performed. The RGB image is converted to HSV and watermarked by using discrete wavelet transform. Watermarking embedded stage and extraction stage is designed using invisible watermarking algorithm. Here the host signal is an image and after embedding the secret data a watermarked image is obtained and then extracts secret image and original image separately. Checking the watermark insertion and quality analysis various parameters like PSNR, Cross correlation etc FPGA implementation of invisible watermarking algorithm using the proposed design can operate at a maximum frequency of 344 MHz .An improvement of 28% in speed has been achieved by consuming considerably less number of resources of Vertex 6 6vsx315tff1156-2 FPGA device to provide cost effective solutions for real time image processing applications.

**Index Terms—** Digital Watermarking, DWT, Invisible Watermarking, Copyright Protection

## 1 INTRODUCTION

The process of digital watermarking involves the modification of the original multimedia data to embed a watermark containing key information such as authentication or copyright codes. The embedding method must leave the original data perceptually unchanged[1]. The major technical challenge is to design a highly robust digital watermarking technique, which discourages copyright infringement by making the process of watermarking removal tedious and costly. A watermarking algorithm consists of the watermark structure, an embedding algorithm, and an extraction, or a detection algorithm [2]. Invisibility refers to the degree of distortion introduced by the watermark. The literature survey explain robustness is the resistance of an embedded watermark against intentional attacks such as noise. Capacity is the amount of data that can be represented by an embedded watermark [3].The most applicable and accurate method is invisible robust watermarking and that is used in this paper. Watermarking represents an efficient technology for ensuring data integrity and data-origin authenticity. Watermarking the process of embedding data into multimedia element can primarily for copyright protection. Because of its growing popularity, the Discrete Wavelet Transform (DWT) is commonly used in the proposed watermarking scheme increase, area increases so power consumption[6].

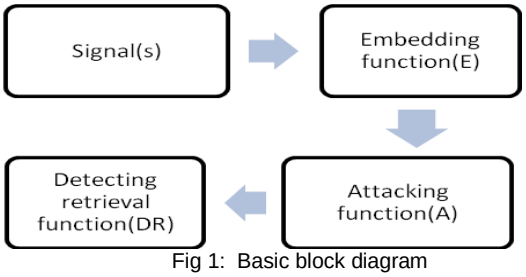

Fig 1: Basic block diagram

## 2 OVERVIEW OF WATERMARKING

A watermarking algorithm consists of the watermark structure, an embedding algorithm, and an extraction, or a detection algorithm. The Xilinx System Generator for DSP is a plug-in to Simulink that enables designers to develop high-performance DSP systems for Xilinx FPGAs. Designers can design and simulate a system using MATLAB, Simulink, and Xilinx library of bit/cycle-true models. The tool will then automatically generate synthesizable Hardware Description Language (HDL) code mapped to Xilinx pre-optimized algorithms[14].In multimedia applications, embedded watermarks should be invisible, robust, and have a high capacity.

Invisibility refers to the degree of distortion introduced by the watermark.

### 2.1 Simulink Block Set

In the VLSI implementation of digital watermarking original image which convert to vector form, then the entire decimal signal are convert to binary signals which means bit form. The group of bits stored in a file and using the simulink block sets read an image in a bit by bit format. The secret image also read in the same.

### 2.2 Xilinx block set

In numerical analysis and functional analysis, a discrete wavelet transform (DWT) is any wavelet transform for which the wavelets are discretely sampled [4]. As with other wavelet transforms, a key advantage it has over Fourier transforms is temporal resolution: it captures both frequency and location information (location in time). Fig 2 shows embedding stage of Invisible robust watermarking algorithm used in simulink and Xilinx block set.

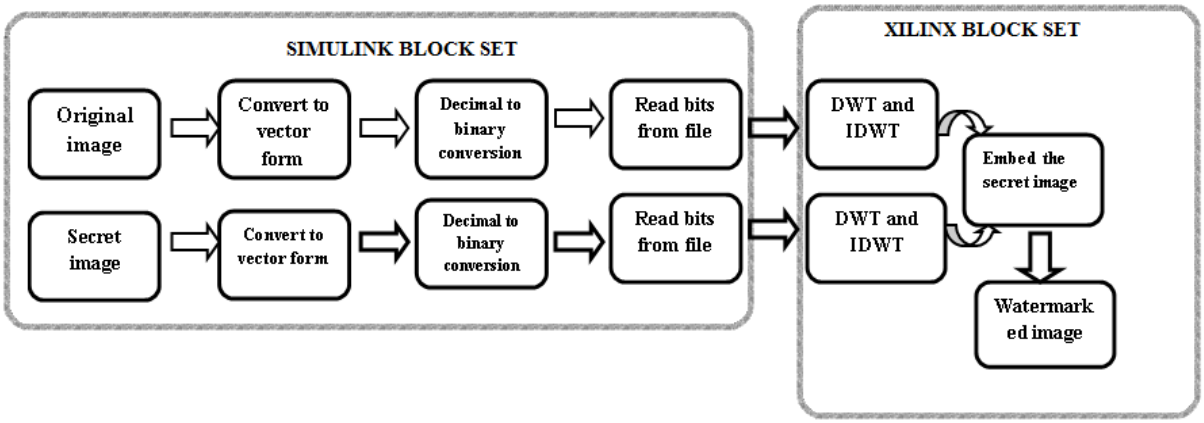


Fig 2: DWT based Embedding stage

The discrete wavelet transform has a huge number of applications in science, engineering, mathematics and computer science [5]. The DWT of a signal x is calculated by passing it through a series of filters [8]. First the samples are passed through a low pass filter with impulse response g resulting in a convolution of the two:

$$y[n] = (x * g)[n] = \sum_{k=-\infty}^{\infty} x[k]g[n-k].$$

Wavelet Transform. It is easy to implement and reduces the computation time and resources required. The discrete wavelet transform uses filter banks for the construction of the multi resolution time-frequency plane[19].

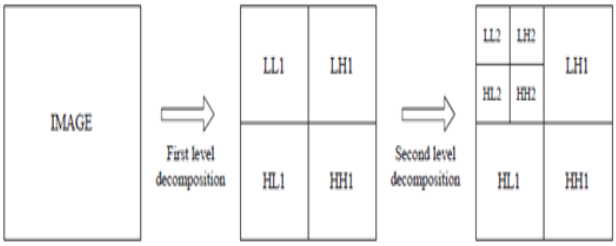


Fig 3 Wavelet decomposition

The Discrete Wavelet Transform analyzes the signal at different frequency bands with different resolutions by decomposing the signal into an approximation and detail information. The decomposition of the signal into different frequency bands obtained by successive high pass g(n) and low pass h(n) filtering of the time domain.

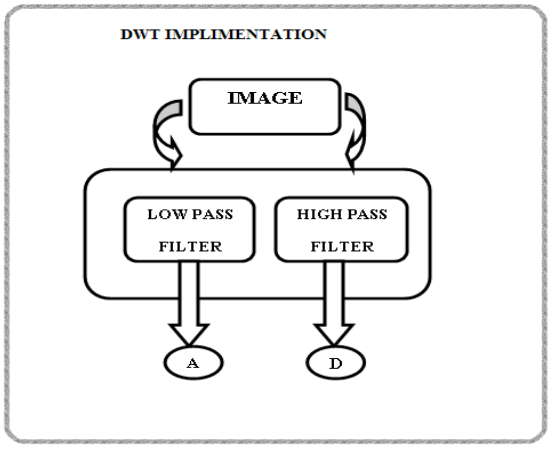


Fig 4 DWT Implementation

The combination of high pass g[n] and low pass filter h[n] comprise a pair of analyzing filters[13]. The o utput of each filter contains half the frequency

content, but an equal amount of samples as the input signal. The fig 4 shows DWT implementation in Xilinx block set.

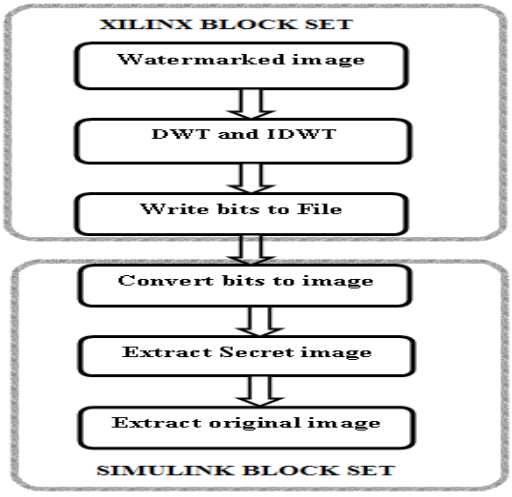


Fig 5: Extraction stage

After the DWT decomposition of secret image and original image embedded the bits from the Secret image in to the original input image bits. Convert the bits in the form of an image using simulink block set and get the Watermarked image .In this work Vertex 6 and Vertex 4 FPGA devices are used for the implementation of Watermarking embedding stage. The extraction stage watermarked image separate out using DWT and IDWT. The group of bits write in to a file and convert bit to image using simulink block set. The watermark must be able to be easily and securely embedded and retrieved by the owner. In this work Vertex 6 and Vertex 4 FPGA devices are used for the implementation of Watermarking extraction stage.

## 3 RESULTS AND DISCUSSION

### 3.1 FPGA Implementation

Model-Based Design to target FPGAs or ASICs can design and simulate systems with MATLAB Simulink and Stateflow and then generate bit-true, cycle-accurate, synthesizable Verilog and VHDL code using Simulink HDL Coder. They can then use Xilinx System Generator for DSP, a plug-in to Simulink code generation software, to automatically generate synthesizable hardware description language (HDL) code mapped to pre-optimized Xilinx algorithms.. The Xilinx System Generator for DSP is a plug-in to Simulink that enables designers to develop high-performance DSP systems for Xilinx FPGAs. Additionally, it provides automatic generation of a HDL testbench, which enables design verification upon implementation.
System Generator works within the Simulink model-based design methodology. The proposed model has designed and simulated using Simulink and Xilinx System Generator block sets. The simulated has been accomplished by using DWT filter in the proposed model. The cameraman image shown in fig 5 is the input image. [256×256] dimensional matrix is represented as input image, which is a gray scale image. The cameraman image converted to vector format and then decimal to binary conversion also done. In multimedia applications, embedded watermarks should be invisible, robust, and have a high capacity. In this case MCK image shown in Fig 6 used as secret image. MCK image is [256×256] dimensional matrix and which convert to vector form. The decimal values converted to binary format. The Xilinx block set read image in the bit form. The discrete wavelet transformed output of secret image and that DWT output of Secret image shown in Fig 7 will embed in to DWT output part of the cameraman image shows in fig 8. The DWT filter uses high pass and low pass filter to decompose the image into its detail and approximate information respectively. 2D-DWT is applied on grayscale image which is shown in figure 7 and 8. It transforms an image into sub-bands such that the wavelet coefficients in the lower level sub-bands typically contain more energy than those in higher level sub-bands.


Fig 6 Input cameraman image


Fig 7.Secret image

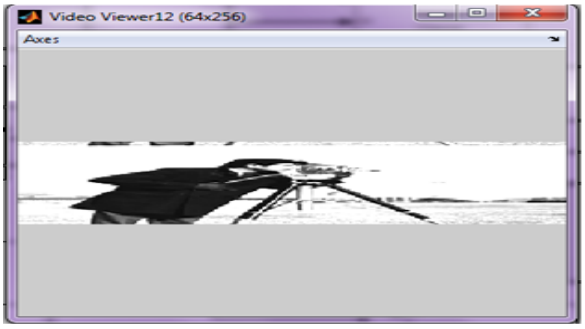


Fig 8. DWT of cameraman image

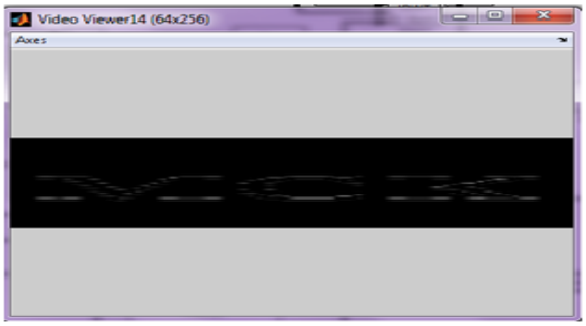


Fig 9.DWT of Secret image

It can be accomplished by applying one-dimensional DWT filter in a separable manner[13]. The first stage of the DWT divides an image into four sub-bands by applying low-pass and high pass filters. The first level of decomposition is consists of two steps. In the first step, each row of an image is transformed using a 1D vertical analysis filter bank. The first step is shown in figure 3. In the second step of the first level of decomposition, each column of the transformed image is again transformed using same filter bank horizontally. The second step is shown in figure 3. Each row and column of the lowest sub-band has been replaced by 1D-DWT. The result of the second level of decomposition has been shown in figure 8 and 9.The discrete wavelet transformed output of secret MCK image and that DWT output of Secret image shown in Fig 9 will embed in to DWT output part of the cameraman image shown in Fig 8.


Fig 10. Watermarked cameraman image


Fig 11.Recovered secret image


Fig 12.Recovered cameraman image

### 3.2 Synthesis results

The synthesizer converts HDL (VHDL/Verilog) code into a gate-level netlist (represented in the terms of the UNISIM component library, a Xilinx library containing basic primitives). By default Xilinx ISE uses built-in synthesizer XST (Xilinx Synthesis Technology). Other synthesizers can also be used. Xilinx 12.1 version is used to synthesis the entire design. The synthesis report allows to view the results of the netlist-generation synthesis process.

This report contains the results from the synthesis run, including area and timing estimation .The targeted device is Virtex 6. Device utilization summary is available after the compile server completes the synthesizing step of the compilation process. This report contains a summary of the FPGA utilization as estimated during the synthesis of the FPGA. Timing report is available after the compile server completes the mapping step of the compilation process. This report contains a summary of the FPGA clocks, as estimated during the mapping of the FPGA. The following table 1 shows the design summary for entire structure.

TABLE 1: DEVICE UTILIZATION SUMMARY OF INVISIBLE WATERMARKING ALGORITHM

| | |
|---|---|
| Number of Slice Registers | 4708 / 393600 (1% ) |
| Number of Slice LUTs | 3922 / 196800 (1%) |
| Minimum period | 2.904ns |
| Maximum Frequency | 344.329MHz |
| Minimum input arrival time before clock | 0.347ns |
| Maximum output required time after clock | 4.147ns |

The maximum frequency reported is 344.329 MHz for the entire design. Since the specified algorithm provide the higher speed than the existing algorithm ,it gives a minimum period 2.904ns. For the device Virtex 6, the obtained maximum frequency is 344.329MHz.

### 3.3 Performance Analysis

The comparison with existing algorithm is very important for evaluating the efficiency of the proposed design. The comparison is performed on the basis of area requirements, power, operation speed etc. The related works shows that different architectures are introduced for invisible robust watermarking algorithm to get sufficient area requirements, speed, power etc. which are suitable for various applications. Here introduce a Invisible robust watermarking algorithm. The following table 2 shows the comparison of the proposed algorithm with previous works. The high speed reported in the previous works is 4.324ns with maximum frequency of 231.29 MHz[13].The present work gives a high speed of 2.904ns with a maximum frequency of 344.329 MHz. The schematic diagram for the entire architecture is shown in figure 13

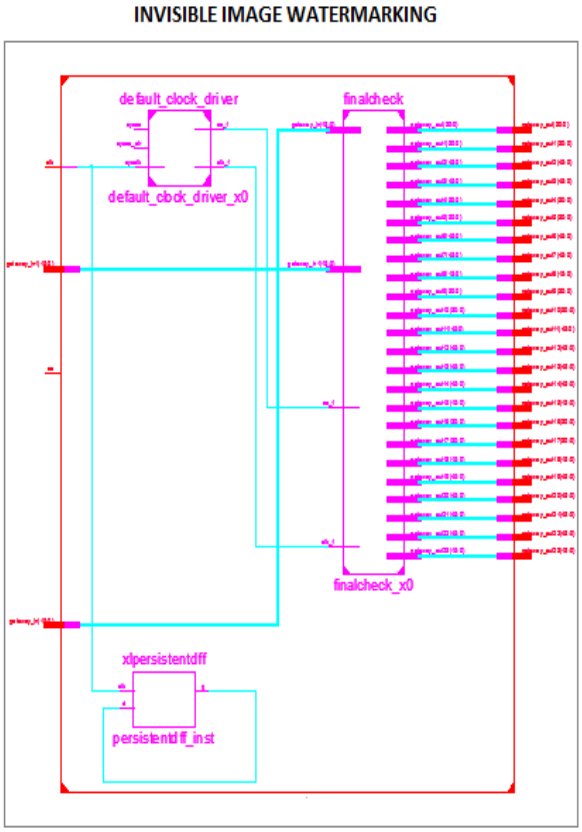


Fig 13: Schematic Diagram of invisible watermarking algorithm

## 4 CONCLUSION

In this Paper, low power high speed and area efficient DWT processor based Image robust watermarking technique for color and gray scale images was performed. The RGB image is converted to HSV and watermarked by using discrete wavelet transform. Watermarking embedded stage and extraction stage is designed using invisible watermarking algorithm. Here the host signal is an image and after embedding the secret data a watermarked image is obtained and then extracts secret image and original image separately. Checking the watermark insertion and quality analysis various parameters like PSNR, Cross correlation etc FPGA implementation of invisible watermarking algorithm using the proposed design can operate at a maximum frequency of 344 MHz .An improvement of 28% in speed has been achieved by consuming considerably less number of resources of Vertex 6 6vsx315tff1156-

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